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(54) Apparatus for synchronising a transceiver with a base station

(57) In a direct sequence spread spectrum code division multiple access (CDMA) communications system, a transceiver 1 can be forced into synchronisation with a broadcast pilot signal from a base station 2 by means of an external synchronisation unit 3 which may be used by an installation operative at the time of deployment of transceiver 1. The unit 3 is synchronised to base station 2 prior to synchronising transceiver 1 and holds this sync state as an operative moves between customer premises. Unit 3 may have a frequency reference which is more accurate than one in transceiver 1. Alternatively, unit 3 may have multiple correlators each able simultaneously and independently to search for a code phase corresponding to a different frequency offset, or able to search many code phases in parallel. To effect carrier frequency lock, a reference frequency oscillator (4, Fig. 2) in unit 3 may be connected to an input of a phase comparator (6) in a phase lock loop in transceiver 1. To provide code phase lock, an output from a linear feedback shift register (10, Fig. 3) in unit 3 may be connected to load a chip sequence into a linear feedback shift register (12) in transceiver 1.

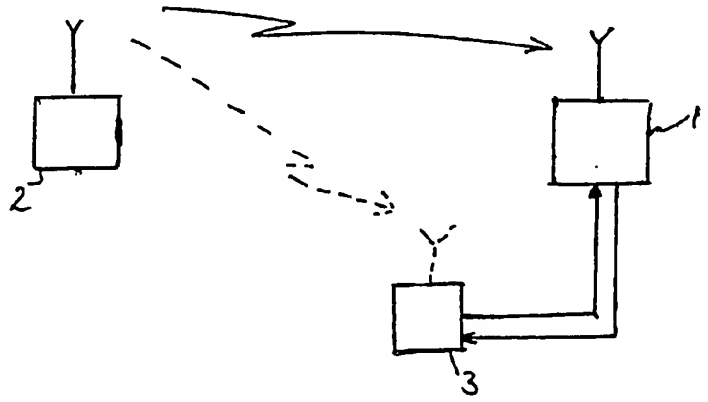

Fig. 1.

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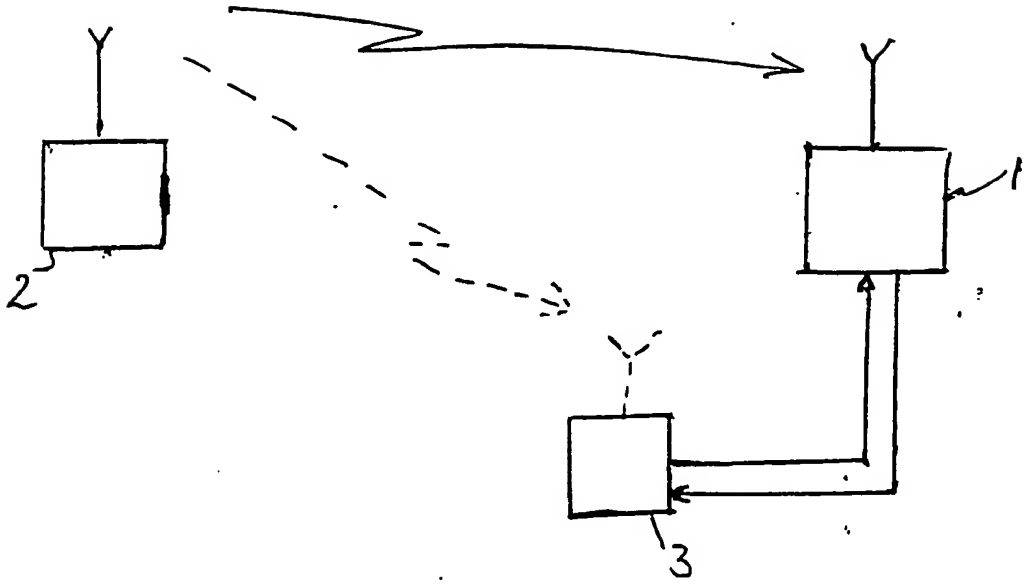

Fig. 1.

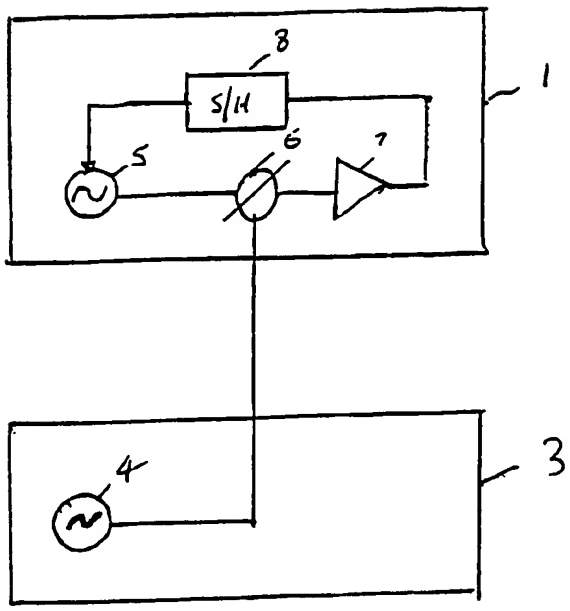

Fig 2

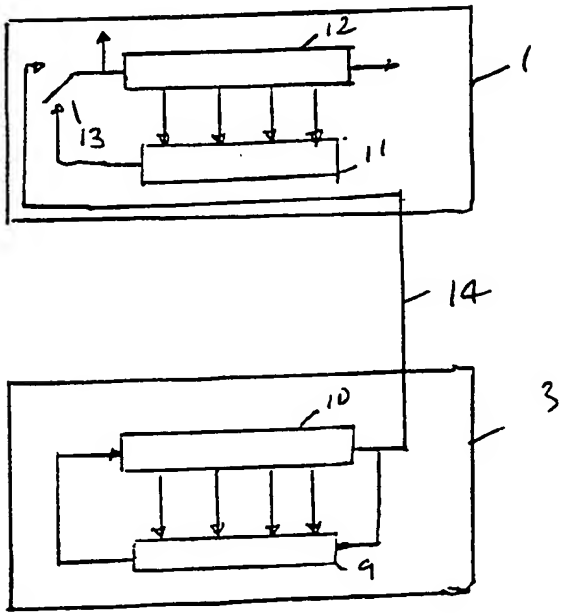

Fig 3

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SYNCHRONISATION APPARATUS

The present invention relates to synchronisation apparatus and in particular to apparatus for synchronising a transceiver with a base station.

The present invention makes use of direct sequence spread spectrum CDMA technology for providing a set of radio links from local exchange to customer premises to provide basic telecommunication type services.

Direct sequence spread spectrum systems generally require synchronisation with carrier phase locking for the transmitted signal and also code phase locking. In the downlink, that is the base station to customer premises equipment direction, a pilot transmission is continuously emitted from the base station, thus the customer premises equipment can be expected to remain in synchronisation both in carrier frequency lock and code phase lock for indefinite periods as long as they are switched on.

The present invention is concerned with the initial acquisition of synchronisation. There are two situations under which this will be required, one is at the time of initial installation and the other is following a power failure which is unsuccessfully bridged by battery backup. It is assumed that the latter case can be covered by synchronisation contained within the radio which is relatively time consuming, however, in the case of initial installation which will likely be performed by an operative of the operating company, long times to achieve synchronisation would prove costly and therefore unacceptable.

An aim of the present invention is to provide rapid synchronisation without the need for expensive equipment contained within the transceiver installed at the customer premises.

According to the present invention there is provided synchronisation apparatus comprising first means located in a transceiver and second means arranged to be connected to the transceiver, said transceiver being arranged to communicate with a base station in a direct sequence spread spectrum CDMA environment, said first means being arranged to force the transceiver into synchronism with the base station when said second means is activated.

A further aspect of the invention requires the second means to include a frequency reference which is more accurate than a frequency reference within the transceiver.

Yet a further aspect of the invention requires the second means to include multiple correlators, each able simultaneously and independently to search for a code phase corresponding to a different frequency offset, or able to search many code phases in parallel.

Still yet a further aspect of the invention is that the second means may be synchronised to the base station prior to conducting the synchronisation process, and has means for holding this synchronisation state as an operative moves between customer premises.

An embodiment of the present invention will now be described with reference to the accompanying drawing, wherein;

FIGURE 1 shows a block diagram of a communication system,

FIGURE 2 shows a block diagram of means for forcing carrier frequency synchronisation, and

FIGURE 3 shows a block diagram of means for forcing code phase lock.

Referring to Figure 1, synchronisation capability of the transceiver 1 should be modest and take a significant period of time, several minutes, but the synchronisation state of the transceiver should be forcible to become synchronised to the broadcast pilot signal from the base station 2 by means of an external synchronisation unit 3 which will be used by the installation operative at the time of deployment of the equipment. Thus, a small number of synchronising units external to the transceivers will be manufactured and these units will achieve rapid synchronisation for the transceivers whenever necessary. The unit 3 will be more complex than the transceiver 1, but being fewer in number, the cost will be acceptable.

There are, as mentioned above, two parts to synchronisation, one is achieving frequency lock such that the code phase shift during the correlation period of the spreading code is acceptably small, and the other is achieving code phase lock.

In general the speed to synchronise both of these is in direct proportion to the cost and complexity of the hardware involved. There are trade-offs in the design of such a synchroniser. The operations involved in a transceiver 1 can be divided into the RF processing and the baseband processing and there is a trade-off between the complexity involved in both of these. If, in the RF

processing the basic frequency accuracy is very good, then less searching needs to be performed in the baseband processing. Therefore one option is to use a much more accurate frequency reference within the synchronisation unit 3 than within the basic customer premises transceiver 1 as shown in Figure 2. Thus synchronisation will be achieved more rapidly by the fact that there will be no need to search across many different frequency intervals. Alternatively, parallel hardware in the baseband processing element of the synchronisation unit, that is to say multiple correlators each able simultaneously and independently to search the code phase corresponding to a different frequency offset could achieve the required effect, or multiple correlators able to search many code phases in parallel may be used, making it possible to rapidly search across all frequency shifts. A further simplification to the system could be that the external synchronisation unit 3 may in fact have no more complexity than the transceiver 1 but that unit would be synchronised to the base station prior to leaving to conduct the synchronisation process, and would have the ability to hold its state as the operative moved from one place to another. Although the basic frequency accuracy of the unit would not be especially good, because it would remain locked to the base station at all times, or would hold its frequency offset during those periods when it was not receiving the signal from the base unit, it would however be pre-synchronised and therefore the time taken to acquire synchronisation would not be needed. Therefore, within the transceiver 1 of the customer premises equipment there would be

means for forcing the code phase of the internal code generator for various of the rake fingers to agree with the code phases of the synchronising unit and also there would be means for the carrier frequency to be locked to the carrier frequency of the synchronising unit by means of a suitable simple interface.

The synchronisation unit 3 may also have means for direct communication with the base station.

Referring to Figure 2, a block diagram of a circuit is shown which is used to force the carrier frequency of the transceiver 1 into synchronism with the base station 2. The circuitry shown and contained in the transceiver 1 is well known in the art and forms a phase lock loop. The phase lock loop comprises an oscillator 5 connected to a phase comparator 6 the output of which is connected via a circuit 7 to a sample and hold circuit 8. The output of the sample and whole circuit 8 completes the loop back to the oscillator 5. In the synchronising unit 3 there is a oscillator 4 the output of which is connected to a further input of the phase comparator 6. The phase lock loop is therefore forced to operate at the referenced frequency generated by the oscillator 4. The purpose of the sample and hold circuit 8 is to maintain operation of the loop when the connection between the oscillator 4 and the phase comparator 6 is removed.

Referring to Figure 3, to provide a code phase lock the transceiver unit 1 includes a linear feedback shift register 12 having various outputs connected to a logic circuit 11, the output of which is connected back to an input of the linear feedback shift register 12 via a switch 13. The synchronisation unit 3 includes a

linear feedback shift register 10 having various outputs connected to a logic circuit 9, the output of which is connected to an input of the linear feedback shift register 10. A further output of the shift register 10 is connected to a further input of the logic circuit 9 and also to a further input of the switch 13 located in the transceiver 1. The linear feedback shift register 10 generates a chip sequence which is fed via a cable 14 to the switch 13. When the switch is in a first position, the chip sequence is loaded into the linear feedback shift register 12. Once this sequence is loaded in the shift register 12 the switch adopts a second position and the output of the logic circuit 11 is connected to the input of the linear shift register 12 and causes a corresponding code sequence to be generated via the logic circuit 11 for the linear feedback shift register 12.

It will be readily appreciated by those skilled in the art that there are various ways of implementing the forcing of the carrier frequency and also of the code phase lock, all of which will fall within the scope of the present invention.

CLAIMS

1. Synchronisation apparatus comprising first means located in a transceiver and second means arranged to be connected to the transceiver, said transceiver being arranged to communicate with a base station in a direct sequence spread spectrum code division multiple access CDMA environment, said first means being arranged to force the transceiver into synchronism with the base station when said second means is activated.

2. Synchronisation apparatus as claimed in claim 1, wherein said second means includes a frequency reference which is more accurate than a frequency reference within the transceiver.

3. Synchronisation apparatus as claimed in claim 1, wherein said second means includes multiple correlators, each able simultaneously and independently to search for a code phase corresponding to a different frequency offset, or able to search many code phases in parallel.

4. Synchronisation apparatus as claimed in any preceding claim, wherein said second means is synchronised to the base station prior to conducting the synchronisation process and includes means for holding this synchronisation state as an operative moves between customer premises.

5. Synchronisation apparatus as claimed in any preceding claim, wherein said first means includes first forcing means for forcing a carrier frequency of the transceiver into synchronism with the base station, said first forcing means being controlled by said second means.

6. Apparatus as claimed in any preceding claim wherein the first means includes second forcing means for forcing a code phase lock, said second forcing means being controlled by said second means.

7. Apparatus as claimed in claim 5, wherein said first forcing means in said transceiver comprises a phase lock loop which is arranged to be controlled by a reference oscillator in said second means.

8. Apparatus as claimed in claim 6, wherein said second forcing means comprises a linear feedback shift register located in said transceiver, and a linear feedback shift register located in said second means and arranged to generate a chip sequence which is applied to the linear feedback shift register contained in said transceiver.

9. Apparatus as substantially as herein before described with reference to the accompanying drawings.

Patents Act 1977 Examiner's report to the Comptroller under Section 17 he Search report)	Application number GB 9502719.9
Relevant Technical Fields (i) UK Cl (Ed.N) H3A AB; H4L LBSF, LBSX, LDLX, LDSX (ii) Int Cl (Ed.6) H03L 7/10; H04B 1/69, 1/707, 1/713, 7/204, 7/212, 7/216, 7/26; H04J 1/06, 3/06, 13/00; H04L 7/00, 7/04, 7/10	Search Examiner MR M J BILLING Date of completion of Search 24 APRIL 1995
Databases (see below) (i) UK Patent Office collections of GB, EP, WO and US patent specifications. (ii) ONLINE: WPI	Documents considered relevant following a search in respect of Claims :- 1 TO 8

Categories of documents

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P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family; corresponding document.

Category	Identity of document and relevant passages		Relevant to claim(s)
X	EP 0555089 A2	(VICTOR) Figure 7B; column 19 line 1 to column 20 line 14	1 at least
X	US 5111479	(CLARION) Figure 4; column 3 line 23 to column 4 line 15	1 at least
A	US 3982075	(THE POST OFFICE) Figure 1; Abstract	1

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